A Reconfigurable Diagnostic Infrastructure for SoCs

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Abstract

Networks on chip (NoCs) are a scalable interconnect solution for large-scale multiprocessor system on chips (SoCs). However, little attention has been paid so far to the debugging, testing and monitoring support for NoC-based systems. This paper proposes a reconfigurable diagnostic infrastructure for SoCs. The proposed infrastructure consists of retargetable embedded in-circuit emulator (ICE), embedded real-time tracer, power measurement, on-chip network analyzer and on-chip network protocol checker. The retargetable embedded ICE module is parameterized and can integrate with different microprocessor. The embedded real-time tracer compresses the external off-chip storage in real-time. The power measurement module that supports power measurement, analysis and management is provided. The on-chip network analyzer can be performed a cycle accurate or successive trace collection in transaction level abstraction. The on-chip network protocol checker monitors network protocol violations.

1. Introduction

System-on-Chip (SoC) design may reuse the pre-design and pre-verified Intellectual Property (IP) modules to reach the time-to-market requirement and reduce the design complexity. Moreover, the networks on chip (NoCs) are a scalable interconnect solution for large-scale multiprocessor system on chips (SoCs). However, the challenges and difficulties of SoC/NoC debugging, testing, monitoring, and integration problems are not efficiently improved. For this reason, we develop the SoC infrastructure IPs such as IP/SoC/NoC debugging mechanisms and system bus platform for easily integration and debugging. In modern SoC/NoC designs, microprocessors/DSPs play an important role in SoCs.

For a customized microprocessor, designer should also implement the debugging and testing mechanism for that microprocessor, and the common debugging/testing hardware for a microprocessor is JTAG based in-circuit emulator (ICE).

In order to achieve the rapid debugging for a customized microprocessor, we have implemented the retargetable embedded ICE module, which can integrate with different microprocessor architectures by setup proper ICE parameters. ICE can help designer to detect the hardware/software bugs, but is difficult to support dynamic debugging such as collecting the execution traces of software programs for debugging or analyzing. For supporting dynamic debugging, we have implemented the real-time hardware trace compressor that records the dynamic instruction address trace and compresses trace data in real-time. The power measurement is designed to analyze the power consumption of the SoC/NoC development platform. The on-chip network analyzer, which can be allowed to perform accurate, successive, trace collection in an unlimited time and can be used in various components without influencing the operation of the on-chip network. The Protocol checker monitors network protocol violations. A key verification task for today’s system-on-chip designers is to ensure that each component in the system obeys the interconnecting bus protocol. To integrate system modules into an SoC efficiently, the on-chip communication protocol should be defined and adopted widely. In this paper, the popular on-chip bus protocol AMBA is chosen. AMBA has developed by ARM, as our bus platform design. SoC designer can follow the interface definition to integrate IPs with system bus.

2. Diagnostic Mechanisms

The purpose of the proposed infrastructure is to establish the diagnostic services platform in SoC/NoC-based systems. Figure 1 shows an example of a diagnostic infrastructure for an SoC system.
There are several types of reconfigurable diagnostic infrastructure intellectual property (IP) modules:

1) A retargetable embedded in-circuit emulator (ICE) [1]: the retargetable embedded ICE is shown in Figure 2. An ICE is part of development environment for microprocessor-based systems (called target systems). An ICE, while retaining the same functionality as the original microprocessor, provides extra debugging and test mechanisms such as single stepping, break point setting and detection, internal resource monitoring and modification, etc., to support designers in the development and maintenance of the hardware and software of the target systems.

2) An embedded real-time tracer [2]: an embedded real-time tracer can help designer to analyze the program behavior and dynamic program execution flow. It has almost 100% compression rate and can transfer the trace data to off-chip storage at real-time speed.

3) A power measurement [5]: the power measurement platform and execution screen are shown in Figure 3 - Figure 6. The power measurement platform that supports power measurement, analysis and management is provided. The power measurement module provides real-time multi-channel probes to measure power of each device of the SoC. The power analysis module can record and analyze power information statistics for each device of the SoC. The power management module provides trigger signals, and then the hardware and software of the SoC can be dynamically switched according to the related-signals for low power and higher performance SoC designs.
4) An on-chip network analyzer [4]: the on-chip network analyzer is shown in Figure 7. The on-chip network analyzer can be allowed to perform accurate, successive, trace collection in an unlimited time and can be used in various components without influencing the operation of the on-chip network. The approach consists of two phases: timing/signal abstraction phase and trace reducing phase. The on-chip network analyzer provides four parameters for tracing configuration, which are event trigger, tracing mode selection, customized signals to be traced, and control signals combination encoding. The on-chip network analyzer is integrated with ARM EASY (Example AMBA SYstem) environment to demonstrate that can trace bus signals deeply and reduce trace size efficiently.

5) An on-chip network protocol checker: Figure 8 shows the on-chip network protocol checker in the SoC System. The on-chip network protocol checker is shown in Figure 9. The on-chip network protocol checker monitors network protocol violations. A key verification task for today’s SoC designers is to ensure that each component in the system obeys the interconnecting bus protocol. Failure to achieve this can result in poor product quality, ASIC re-spin, and delayed entry into the market with corresponding loss of revenues.
3. Conclusion

In this paper, we introduce five diagnostic infrastructure IP modules that provide debugging, testing and monitoring for SoC-based systems. The proposed infrastructure consists of retargetable embedded in-circuit emulator (ICE), embedded real-time tracer, power measurement, on-chip network analyzer and on-chip network protocol checker. The ratargetable embedded ICE module is parameterized and can integrate with different microprocessors. The embedded real-time tracer compresses the external off-chip storage in real-time. The power measurement module that supports power measurement, analysis and management is provided. The on-chip network analyzer can be performed a cycle accurate or successive trace collection in transaction level abstraction. The on-chip network protocol checker monitors network protocol violations. Such infrastructure is extremely needed for developing complex NoC/SoC-based systems.

4. References


