

DESIGN AND VLSI IMPLEMENTATION OF A DIGITAL AUDIO-SPECIFIC DSP CORE FOR MP3/AAC

Kyoung Ho Bang¹, Nam Hun Jeong², Joon Seok Kim², Young Cheol Park¹ and Dae Hee Youn¹
¹Dept. of Electrical and Electronic Eng., Yonsei University, Seoul, Korea
²InTime Cooperation, Seoul, Korea

ABSTRACT

In this paper, a digital audio-specific DSP core designed for dual MP3/AAC decoder is presented. The processing core is a 20-bit fixed-point programmable DSP having an architecture suitable for audio signal processing. It supports special instructions like UNPACK, HUFFMAN as well as general arithmetic and logical instructions including pipelined-MAC. All instructions are completed within a single cycle. The DSP core is realized in a 0.35 μm 3.3 V CMOS technology and operates at 40MHz. The implemented DSP core with a dedicated hardware accelerator can decode MP3 using only 13.33MIPS and AAC using only 16.9 MIPS with high efficiency.

1 INTRODUCTION

The demands for high-quality digital audio system arise. MPEG/Audio layer-3 (MP3) [1] and MPEG-2 Advanced Audio Coding (AAC) [2][3] are standardized audio compression methods, which become more and more popular in the consumer market due to the high compression ratio and the transparent quality. Similarly, demands on appropriate enabling hardware are also rising. This commonly leads to a hardware system which is partitioned into embedded digital signal processor (DSP) core, application-specific integrated circuits (ASIC) and a micro-controller. Thereby, the DSP cores are often general purpose cores and realize basic signal processing tasks in the system, whereas dedicated hardware is well suited to realize the complex algorithms of the application in a power efficient way. ASIC implementations are limited to separated tasks with neither the opportunity to adopt other tasks nor the

feasibility to modify the actual target algorithm due to changes in it. Hence, modifications in the application lead to a time consuming and error-prone redesign of the dedicated hardware.

Unlike conventional methods, DSP core-based ASIC design combines the benefits of a standard off-the-shelf DSP and optimized custom hardware. In this paper we present our digital audio-specific DSP core which results from the approach of designing application specific DSP with dedicated hardware accelerator.

2 DSP CORE DESIGN

DSP core design is focused on three aspects: suitable for the high-quality audio coding, low power consumption, and easy programming.

First of all, audio coding algorithms, such as MPEG-1/2 Layer II, III, MPEG-2 AAC, and AC-3 [4][5] were analyzed to measure the required accuracy of the implementation processor. The requirement for the processing accuracy was generated from the ISO/IEC 13818-4 compliance [6] and top class equipment [7]. Based on the analysis, desirable specifications for the DSP core was obtained as followings:

- Data processing unit should have
 - 20-bit data, 48-bit ALU, accumulator
 - Multiplier supporting signed by signed, signed by unsigned, unsigned by unsigned multiplications
 - Convergent rounder, and limiter
- More than 18-bit PCM output is desirable

- One cycle MAC operation for efficient processing of F/T transform
- 2048 modulo addressing for management of 2048-sized buffer of AAC
- Efficient implementation of 512-point complex FFT for AC-3 and AAC

For the low power consumption design of hardware architectural level, two methodologies were considered. In order to prevent unnecessary power consumption, a minimum hardware resource should be used. To this end, single ALU architecture was employed. Also, a 3-stage pipelining Harvard architecture was employed for fast instruction flow control. The second consideration was to disable unused hardware resource. To this end, the DSP core was designed to cut off the current flow to unused hardware in an active way. The input cut off method was realized using latch.

For easy programming, the instruction set was designed to provide a maximum degree of freedom for the audio algorithms. Through the operation scheduling and hardware resource allocation, programmer can use full 3-stage pipeline.

3 SYSTEM ARCHITECTURE

Figure 1 shows a block diagram of DSP core architecture. The DSP core consists of three main functional units: instruction fetch unit, instruction decoder unit and execution unit. It has a modified Harvard architecture with six buses. All three main units can access the X and Y data memories through the dedicated X and Y buses. The instruction fetch unit uses separate buses, the PMD and PMA for fetching instruction words. Although data and program memories are mandatory components of all DSP-core-based systems, they are not considered part of the core itself.

The DSP core uses a load-store architecture; that is, operands are loaded into registers before they are processed by the data processing unit. In addition to basic subtraction and addition, the arithmetic logic unit (ALU) supports fundamental bit logic operations. The data processing unit of the DSP core is based on a single MAC architecture. The multiply unit (MU) and ALU can multiply two general purpose registers and sum the result with the previous value in the product register (P reg). Figure 2 shows the data processing unit accommodating a MU, a shifter, and a ALU.

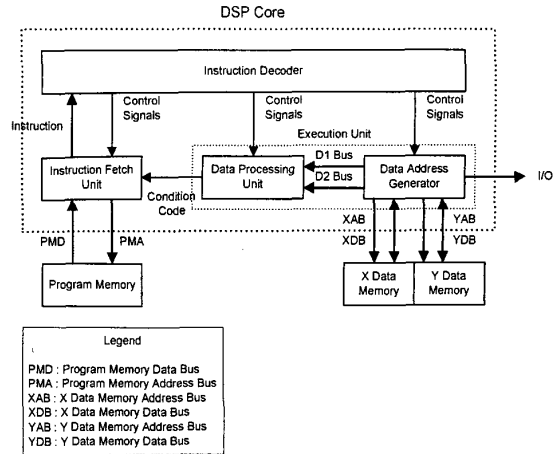


Figure 1. The architecture of DSP core

The data address generator provides data addresses and post-modifies the index registers if necessary. Consisting of an index register file and two identical address calculation units, it generates two independent data addresses on each cycle.

The instruction fetch unit, which consists of the execution control and the instruction address generator, controls operation of all core units and additional off-core functional units. It usually obtains the program memory address from either the program counter, the immediate address of a branch instruction, or a loop instruction.

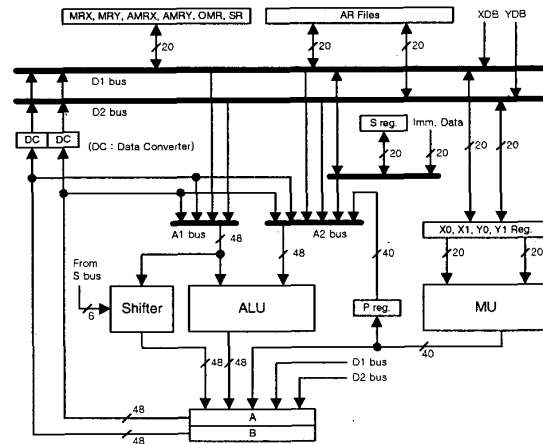


Figure 2. The architecture of data processing unit

The DSP architecture is based on the 3-stage pipeline for low-power design and sufficient for the audio decoding algorithms. The core features a three-stage pipeline - fetch, decode, and execute-and executes instructions effectively in one clock cycle. Instructions causing program flow discontinuity, such as branches, have one delay slot.

4 INSTRUCTION SET

The processing core is programmable using its own assembly language and it supports special instructions like UNPACK, HUFFMAN as well as general arithmetic and logical instructions including pipelined-MAC. Especially, UNPACK is a useful instruction for bit-parsing. All instructions are completed within a single cycle [8].

Table 1 lists the basic instruction set containing 27 instructions, which can be extended to support application-specific features of the data path and additional functional units.

Table 1 Instruction set overview

Mnemonic	Description
ARITHMETIC AND LOGIC	
AND	Logical AND
NOT	Logical NOT
OR	Logical OR
XOR	Logical XOR
ABS	Absolute value
ADD	Add two operands
SUB	Subtract two operands
ASL	Arithmetic shift left
ASR	Arithmetic shift right
CMP	Compare
NEG	2's complement
RND	Round
SAT	Saturation
MULTIPLIER	
MPY	Signed by Signed
MPYSU	Signed by Unsigned
MPYUS	Unsigned by Signed
MPYUU	Unsigned by Unsigned
MOVES	
MOVE X:Reg, Y:Reg	
MOVE X:Reg	

MOVE Y:Reg
MOVE Reg, Reg
MOVE Imm, Reg

CONTROL

BR Unconditional Branch
BRC Conditional Branch
CALL Call subroutine
RET Return from subroutine
LOOP Start a loop

5 SYSTEM EFFICIENCY

The DSP core and hardwired accelerator is designed with VHDL, compiled and simulated by SYNOPSIS tool. The proposed design is implemented in VLSI using 0.35 μm 3.3V CMOS technology.

To verify the implemented system, two verifications were applied to the designed system. First verification was to examine the validation of the MP3/AAC decoding algorithm with the designed system, and second one was to verify the feasibility of the real-time operation for the decoding process.

First, results of the floating-point and fixed-point simulations were compared with each other for the performance evaluation. Simulations were performed using C language programs in the algorithm design stage. The floating-point simulation was for the verification of the MP3/AAC decoding algorithm and the fixed-point one was concerned with reducing the error due to the finite word-length restriction. The requirements of ISO/IEC 13818-4 compliance test [6] are that noise level (NL) be less than -101dB FS and maximum error ratio (MER) be less than 1. The performance of the implemented system is shown in Table 2 and Table 3. N_p is the number of processing bit and N_o is the number of output PCM bit.

Table 2. Quality test of the designed system (MP3 decoder)

N_p	$N_o = N_p$		$N_o = 16$		$N_o = 20$	
	NL	MER	NL	MER	NL	MER
16	-81.3	7.18	-81.3	7.18	-81.3	7.19
18	-92.0	2.00	-91.5	2.25	-92.0	2.00
20	-100.3	1.09	-97.7	1.06	-100.3	1.09
22	-110.0	0.24	-100.8	0.44	-109.9	0.25
24	-117.8	0.10	-101.2	0.33	-117.1	0.11

Table 3. Quality test of the designed system (AAC decoder)

Np	No = Np		No = 16		No = 20	
	NL	MER	NL	MER	NL	MER
16	-85.6	5.05	-85.6	5.05	-85.6	5.05
18	-94.6	2.27	-94.0	2.33	-94.6	2.27
20	-100.2	1.11	-97.8	1.25	-100.2	1.11
22	-109.8	0.64	-100.9	0.64	-109.7	0.64
24	-118.1	0.64	-101.3	0.64	-117.3	0.64

The verification of real-time decoding was carried by comparing the number of the clock cycles in the worst simulation case with the required clock cycles for the real-time decoding. For these two verifications, we used the C language-based simulator of the DSP core. When 48kHz sampling frequency is considered and the processing core operates at 40MHz, the number of clock cycles for decoding one time sample in real-time is

$$f_{clk} \times \frac{1}{F_s} = 40 \times 10^6 \times \frac{1}{48 \times 10^3} = 833.3 (\text{cycles})$$

Therefore, the decoding system must finish the each MP3/AAC decoding process in less than 853,299 and 960,000 clock cycles a frame. Table 4 and Table 5 summarize the required clock cycles in each decoding step. The designed MP3/AAC decoding system consumes less than 348,406 cycles (13.33 MIPS) and 361,828 cycles (16.90 MIPS) each to decode one frame of MP3 and AAC data, respectively. For the results of Table 4 and Table 5, worst simulation case was considered. The results show that the designed system is very efficient in MIPS for decoding MP3/AAC bitstreams in real-time, but it is still with high audio quality. The complexity of the implemented system is summarized in Table 6. The proposed design is implemented in VLSI using 0.35 μ m 3.3V CMOS technology and the gate count of the system is summarized in Table 7. This decoding system uses less memory resource, clock cycles, and complexity than other cases can be found in [9] [10].

Table 4. Clock cycles for decoding MP3 bitstream

Decoding process	Number of cycles	MIPS
Noiseless decoding	106,646	4.08
Stereo	11,288	0.43
IMDCT	74,548	2.85
Subband filtering	155,924	5.97
Total sum	348,406	13.33

Table 5. Clock cycles for decoding AAC bitstream

Decoding process	Number of cycles	MIPS
Noiseless decoding	112,140	5.26
Stereo	13,560	0.64
Prediction	15,430	0.65
TNS	105,370	4.94
Filter bank	115,328	5.41
Total sum	361,828	16.90

Table 6. Memory requirement of MP3/AAC system

	H/W Resource	Size (word)
MP3	Program Memory	2.2k
	Data ROM	1.4 k
	Data RAM	5.7k
AAC	Program Memory	4.1k
	Data ROM	5.5k
	Data RAM	7.1k

Table 7. The gate count of dual MP3/AAC decoder

Module	Gate Count
DSP Core	23145.0
AAC Huffman Decoder	3987.5
MP3 Huffman Decoder	4574.0
Predictor	5760.8

6 CONCLUSIONS

We have designed a digital audio-specific DSP core for dual MP3/AAC decoder. The implemented system consists of a 20-bit fixed-point DSP core for the software implementation and a hardware accelerator. Dual MP3/AAC decoding system can decode MP3 using only 13.33 MIPS and AAC using only 16.9 MIPS with high efficiency. Therefore the designed DSP core is suitable for the digital audio signal processing. Figure 3 depicts the system evaluation board for dual MP3/AAC decoding system embedded DSP core.

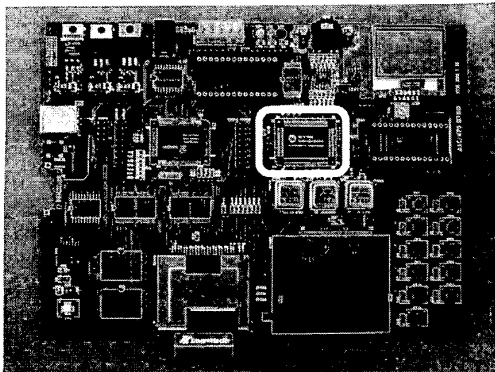


Figure 3. Evaluation board for dual MP3/AAC decoding system embedded DSP core

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BIOGRAPHY



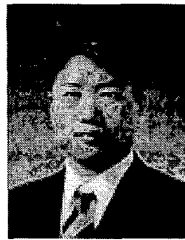
Kyoung Ho Bang was born in Pohang, Korea, on October 22, 1976. He received his B.S. and M.S. degrees in Electronic Engineering from Yonsei University, Seoul, Korea in 1999 and 2001 respectively.

He is currently a Ph.D. candidate in Department of Electrical and Electronic Engineering at Yonsei University, Seoul, Korea. His research interests include audio signal processing, DSP & ASIC implementation, high quality audio coding, HDL chip design, and algorithm optimization.



Nam Hun Jeong was born in Namwon, Korea, in 1973. He received his B.S., M.S., and Ph.D. degrees in Electronic Engineering from Yonsei University, Seoul, Korea in 1995, 1997, and 2001 respectively.

In 2001 he joined the InTime Corp. in Seoul, Korea, where he works as a research engineer in VoIP group. His areas of interest are algorithms for digital audio processing, $\Sigma - \Delta$ modulation, and adaptive digital filter design with a special focus on HDL chip design.



Joon Seok Kim was born in Seoul, Korea in 1972. He received his B.S., M.S., and Ph.D. degrees in Electronic Engineering from Yonsei University, Seoul, Korea in 1995, 1997, and 2001 respectively.

In 2001 he joined the InTime Corp. in Seoul, Korea, where he works as a research engineer in VoIP group. His areas of interest are algorithms for digital audio processing, ADSL and 3D audio with a special focus on DSP core design.



Young Cheol Park received his B.S., M.S., and Ph.D. degrees in Electronic Engineering from Yonsei University, Seoul, Korea in 1986, 1988, and 1993 respectively.

From 1993 to 1995, he was a Post Doctoral Research Scholar of the graduate program in acoustics in Pennsylvania State University, PA, USA. From 1996 to 1998, he was with Samsung Electronics Co., Ltd., Kiheung Korea, working on the development of digital hearing aids. In 1999 he joined InTime Corp. in Seoul, Korea. His research interests include digital audio, speech coding, and adaptive filters. He is also a staff member of the Center for Signal Processing Research (CSPR), Yonsei University, Seoul, Korea.



Dae Hee Youn received his B.S. degree in Electronic Engineering from Yonsei University, Seoul, Korea, in 1977, and the M.S. and Ph.D. degrees in Electrical Engineering from Kansas State University, Manhattan, Kansas, in 1979 and 1982, respectively.

From 1982 to 1985, he was an assistant professor at the University of Iowa, Iowa City, Iowa. Since 1985, he has been with the Department of Electrical and Electronic Engineering at Yonsei University, Seoul, Korea, where he is currently a professor. His research interests include adaptive digital filter and its application, speech and audio signal processing, and real-time implementation of DSP algorithms.