ANATOMY OF A PORTABLE DIGITAL MEDIAPROCESSOR


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Abstract

Portable devices equipped with imaging, video, and audio functionality are proliferating rapidly. Manufactures also require faster time to market, flexibility, and low overall system cost. To meet requirements and reduce overall cost, media processor designers must integrate the device with an extensive set of peripherals. This article discusses the architecture of the DM310, a highly integrated portable digital media processor.
What’s the problem?

- The key features of current high-end embedded products
  - Multi-function (image, video, audio)
  - Faster time-to-market (flexibility)
  - Low cost

- EX: Cell phone, PDA, MP3 player…..
DM310 processor

- Imaging/video
- Digital signal processor (DSP)
- Coprocessor
- ARM subsystem
Block diagram of the DM310 digital mediaprocessor

- Imaging/video subsystem
  - CCD/CMOS imager
  - CCD controller
  - Preview engine
  - SDRAM
  - DACs
  - Video encoder
  - OSD
  - USBF
  - USBH
  - GIO
  - UART
  - MMC/SD
  - MemStick
  - WDT
  - External memory I/F for CFC/SM Flash/SRAM
  - ARM925
  - 16-Kbyte instruction cache
  - 8-Kbyte data cache
  - 8-Kbyte RAM

- DSP subsystem
  - DSP (C54x) core
  - 128-Kbyte RAM
  - Image buffers (31 K-entries × 16 bits)
  - Quantization and inverse quantization
  - Variable-length coder and decoder

- ARM subsystem
  - Coprocessor subsystem

- Analog/digital, digital/analog serial interface for audio
Imaging/video subsystem

- Preview engine:
  1. perform noise filtering
  2. white balance
  3. gamma correction
  4. color conversion from RGB to YUV
Imaging/video subsystem (cont.)

- OSD (on-screen display) block:
  support menu and video window display

- Video encoder:
  display the OSD output on an analog NTSC/PAL display and a digital LCD
Block diagram of the DM310 digital media processor
DSP subsystem

- Texas Instruments TMS320C54x core with 128 Kbytes of program/data RAM operating at a maximum of 72 MHz

- The DSP works closely in conjunction with the coprocessor subsystem to execute the bulk of the audio/image/video processing computations
Block diagram of the DM310 digital mediaprocessor

- Imaging/video subsystem
  - CCD/CMOS imager
  - Preview engine
  - Video encoder
  - OSD
  - DACs
  - SDRAM
  - CCD controller
  - SDRAM/memory traffic controller

- ARM subsystem
  - USBF
  - USBH
  - GPIO
  - UART
  - MMC/SD
  - MemStick
  - WDT
  - External memory
  - I/F for CFC/SM
  - Flash/SRAM
  - ARM925
    - 16-Kbyte instruction cache
    - 8-Kbyte data cache
    - 8-Kbyte RAM

- Coprocessor subsystem
  - Variable-length coder and decoder
  - Quantization and inverse quantization
  - Imaging accelerator (iMx)
  - 128-Kbyte RAM
  - DSP (C54x) core

- Analog/digital, digital/analog serial interface for audio
Coprocessor subsystem

- Contain three component:

  1. Imaging accelerator (iMX)
  2. Quantization and inverse quantization (QiQ)
     - Accelerate several image/video compression algorithm.
  3. Variable-length coder and decoder
     - Accelerates Huffman coding and compression.
Imaging accelerator (iMX)

- Eight-way single-instruction, multiple-data (SIMD)
- Works on either 8 or 16 bit data.
- To accelerate image/video algorithm.
- Supports arithmetic and logical operations.
Question?

- Why a DSP core has multiple coprocessors instead of having a single processor in the DM310?

**Ans:**

1. The coprocessors and the DSP core run concurrently on different parts of the algorithm. The DM310 can execute three threads of concurrency in the DSP and coprocessor subsystem.

2. Having a dual-core architecture (DSP and ARM) allows a clear separation and abstraction of the multimedia tasks from the system tasks.
ARM subsystem

- ARM925 processor with 16 Kbytes instruction caching and 8 Kbytes of data caching
- Do most system-level tasks and control all the components on chip except the DSP and the coprocessor subsystem.
Performance and Power Results

- **Performance**
  - The DM310’s performance specifications call for real-time (30 frames/s) MPEG-1 and MPEG-4 video encoding at CIF (common intermediate format) resolution (352x288 pixels) and real-time (30 frames/s) MPEG-1 and MPEG-4 video decoding at VGA resolution.

- **Power**
  - Encoding and decoding consumes 400mW for the whole chip
  - Capturing a still image (processing 6 megapixels per second, including JPEG compression), consumes 400 mW
Example Application

- Vertical drive
- SDRAM
- NAND flash
- EPROM/flash
- Speaker output
- Microphone voice input
- Secure Digital card
- Color LCD panel
- Real-time-clock battery
- To digital still camera engine
- Crystals

- Optical filter
- Lens module
- CCD/CMOS sensor
- Lens motor drivers
- Analog front end
- Timing generators
- Horizontal drive
- Strobe module
- Power management/battery charge circuit
- System batteries

DM310 as the digital still camera engine

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Conclusions

- This article presents a high-integrated media-processor for low-cost portable device
  - ARM subsystem
  - DSP subsystem
  - Imaging/Video subsystem
  - Coprocessor subsystem

- Three on-chip phase-locked loops (PLLs) control the DM310’s clocking scheme.
  - Several possible clock frequencies run on different portions of the chip

- Use thread to speed the throughput.