BSM2: Next Generation Boundary-Scan Master

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Boundary-Scan Master

- The **boundary-scan master** chip used for a parallel-serial interface between a service processor and boards.
What’s the Problem?

- Improved the performance and capability compared with original BSM.
- Incorporated new operational modes and feature
- Provide higher-level user interface
Introduction

- BSM2 is a new ASIC device
- Can be used in TAP-based DSP application areas

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<tr>
<th>Category</th>
<th>Device 497AE</th>
<th>Device 1215E</th>
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<td>Operation Modes</td>
<td>1. 497AA Compatibility Mode</td>
<td>Advanced Operational Mode</td>
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<td>2. Advanced Operational Mode</td>
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<td>Host Interface</td>
<td>1. Old 8-bit synchronous interface</td>
<td>New 16-bit asynchronous interface</td>
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<td>2. New 8-bit asynchronous interface</td>
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<td>Register Access</td>
<td>Indirect Addressing Method</td>
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<td>Voltage &amp; Frequency</td>
<td>3.3 V supply &amp; 65 MHz Clock</td>
<td>3.3V supply &amp; 65 MHz Clock</td>
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<td>Technology</td>
<td>Lucent 0.35 μ CMOS process</td>
<td>Lucent 0.35 μ CMOS process</td>
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<td>Package</td>
<td>28-pin SOJ package</td>
<td>48-pin TQFP package</td>
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Operation
(briefly introduction)

- Operate in two modes
  - An old mode: compatibility mode
  - A new mode: advanced operational mode
BSM2: Architecture
Host Interface

- Parallel / Serial converter
- Provides generic control functions
  - Chip enable
  - Read/write control
  - Data available/valid
  - Interrupt signals
BSM2: Architecture
Device Controller

- Provides high-level coordination and synchronization
- Controls the registers and memories states
  - Execute, jump, reset
- TCK signal
  - Auto-pause mode: free running
  - Gated-TCK mode: TCK is disabled until the execution is enable
BSM2: Architecture
TVI / TVO Memories

- Consists of 8K bits organized as 512 16-bit words
- During normal mode
  - Behave as FIFOs
  - Scan length: depends on internal scan counter
- During ATPG mode
  - Each memory location can be addressed individually for read and write operations
  - Scan lengths: 8K
TCK Generator and Gating

- The TCK generator can be programmed to divide the input master clock by $2^n$, $n \in \mathbb{N}, 0 \leq n \leq 7$

- In gated-TCK mode
  - TCK running: when scanning or state change
  - TCK gated off: TAP state machine reaches the destination state or memory overflow/underflow
BSM2: Architecture
TMS Generator

- In the normal mode, TMS generated based on (automatic TMS generator)
  - The current state
  - The desired state
  - The desired idle operation
  - The destination state

- Overflow/underflow -> shift-IR/DR state
BSM2: Architecture
ATPG and SAR

- ATPG and SA registers are used to test
  - Interconnect test between UUT devices
    » Walking one/zero sequence
  - Cluster test of non-B-S devices and Internal logic of UUT devices
    » Pseudo-random sequence

| 1 0 0 0 |
| 0 1 0 0 |
| 0 1 0 0 |
| 0 0 1 0 |
| 0 0 0 1 |

Walking one sequence
Hardware and Software Co-Verification

- An existing software suite and BSM hardware design
- H/W and S/W co-simulation tool to integrate the RTL code of the BSM2 device with a virtual s/w processor
BSM Applications

- Digital Signal Processing application

- System-on-Chip designs
  - TAP can be controlled by the BSM2 to deliver the protocols to provide access to the internal cores
Conclusion

- Provides a more flexible architecture and higher level user interface for board/system designers.
- Widely used for boundary-scan applications.