The IEEE P1500 Embedded Core Test

Presented by
Wei Chen, Wang
Presentation Outline

- Introduction
- Overview of Proposed Architecture
  - System chip with P1500 cores
- Core Test Requirements
- P1500 Architecture Components
  - Core test wrapper components
  - P1500 protocol and behavior
- Example
Introduction

- IEEE Std. 1149.1 TAP and boundary scan
  - Well known
- IEEE P1500 wrapper
  - Define a core test interface between an embedded core and the system chip
  - Facilitate test reuse for embedded cores through core access and isolation mechanism
Overview of P1500 Architecture

System chip with P1500 cores

0 to n lines for parallel and/or serial test data, or test control

From chip I/O and from test bus

From chip I/O and from test bus
P1500 Core Test Requirements

Proposed Core Test Wrapper Modes

- **Normal**
  - Allows core to function in its normal system operation

- **Core-Internal Test**
  - Allows the internal core logic to be tested via the core test wrapper

- **Core-External Test**
  - Allows testing of interconnect wiring and logic between cores via the core test wrapper

- **Isolation**
  - Allows the core to be isolated, in a safe state, in order to facilitate testing of other cores and non-core chip logic
P1500 Core Test Requirements

Test Functions at Core Terminals

- Input Test Functions
  - Observation
  - Control

- Output Test Functions
  - Observation
  - Control
  - Disable
A P1500 wrapper contains the following:
- A Wrapper Instruction Register for providing wrapper mode control
- Wrapper Cells to provide test functions at the core terminals
- An serial interface for providing initialization and communication to the WrapperInstruction Register, Wrapper Cells, and Bypass register

The Bypass register is an optional component
P1500 Wrapper Instruction Register

Proposed Required Instructions

- Normal
- Core Test 1-N
  - Wrapper cells are connected to TAM and/or wrapper serial input/output for core test
  - Sources & sinks, 1-N, and core test methods are user defined
- Serial External Test
  - Wrapper cells are connected serially between the wrapper serial input/output
- Isolation
  - Wrapper cells enable setting of appropriate core I/Os to constrained and/or disabled values for core isolation
Standard P1500 protocol for Wrapper Registers will provided for:
- Update scan-in data of register to a parallel update stage
  » Required for Wrapper Instruction Register and optional for others
P1500 Wrapper Registers

Standard Serial Scan Path Configuration

1. Serial input to Wrapper Instruction Register (WIR) or other Data Registers (DRs), e.g. Wrapper Cell Register, Bypass, etc.

2. Update WIR then selects between DRs

Core test 1-N instructions permit TAM connection & configuration of Wrapper DRs, or internal core registers, to be used defined!
P1500 Wrapper Cell Example
Dedicated Output Cell with Update Stage & TAM-Out

Cell behavior in response to Wrapper Instructions

- **Normal**: Cell output connects to Cell input
- **Serial External Test**: Cell output is sourced from cell’s update stage
- **Isolation**: Cell output is appropriately disabled or constrained
- **Core Test 1**: TAM-Out is sink & provides output observation for core test
Cell behavior in response to Wrapper Instructions

- **Normal**: Cell output connects to Cell input
- **Serial External Test**: Cell input is captured into cell’s shift stage
- **Isolation**: Cell output is appropriately constrained
- **Core Test 1**: TAM-In is source & provides input control for core test
Core internal scan paths & Wrapper Cell Register are connected in parallel to TAM by a Core Test instruction.

Many other TAM connections and configurations are possible.